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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/604,301	06/26/2000	Yusuke Tsutsui	81784.0210	3587

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EXAMINER
NGUYEN, HAU H

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/604,301	Applicant(s) TSUTSUI ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *5 and 13-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 recites the limitation "the 400th, 320th, and 256th data items" in page 72, line 11. There is insufficient antecedent basis for this limitation in the claim. It appears that claim 6 is dependent on claim 5. Claim 7 is dependent on claim 6 is thus rejected.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 2, 8, 10 are rejected under 35 U.S.C. 102(a) as being anticipated by Mano et al. (U.S. Patent No. 4,985,698).

Referring to claims 1, 2 and 10, Mano et al. teach a display panel driving apparatus of the present invention including a column-direction drive circuit, which is divided into N drive circuits. Further, a line memory having a memory capacity corresponding to one line is connected to the column-direction drive circuit. As in the case of the column-direction drive circuit divided into the N drive circuits, the line memory is also divided into N memory regions, and its i-th memory region (i =<N) is connected to the i-th drive circuit. Picture data are stored in the sequential order from the first region to the N-th region of the line memory. At the time

where picture data of one line are completely stored in the line memory, the picture data are transferred from the individual memory regions to the associated drive circuits respectively. This data transfer is such that the data are simultaneously transferred from the individual regions of the line memory to the associated column-direction drive circuits respectively. Alternatively, the picture data are transferred sequentially or serially at a high speed in a relation divided into units (col. 2, lines 22-42). With reference to Fig. 1, data are selectively supplied through the multiplexer MPX 2 (a memory selection circuit) to a write input terminal of a first line memory 3 and a write input terminal of a second line memory 4 (col. 3, lines 45-49), and output to a read memory selection circuit MPX 5, which is connected to read output terminals of the first and second line memories 3 and 4 (col. 4, lines 14-16). As shown in Fig. 1, Mano et al. further teach a divided data control circuit DDC 8 receives 4-bit data to be displayed on the left-hand display area and 4-bit data to be displayed on the right-hand display area and supplies the former and latter data to the left-hand and right-hand X drive circuits XDVL 9 and XDVR 10 respectively (col. 5, lines 13-17).

In regard to claim 8, Mano et al. further teach each of the first and second line memories 3 and 4 has a memory capacity capable of storing color display data corresponding to one line of the color liquid crystal display panel LCD 11. That is, a memory capacity of 640 dots X 3 color bits is required for each of the first and second line memories 3 and 4 because the color liquid crystal display panel LCD 11 has the display capacity of 640 dots in the horizontal direction (col. 3, lines 50-56).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 102(a) as being anticipated by Mano et al. (U.S. Patent No. 4,985,698).

Referring to claim 5, as applied to claim 1 above, Mano et al. teach all the limitations of claim 5, except for the data storage capacities of the input and output line memory correspond to 400 pixels or 512 pixels. However, it would have been an obvious matter of design choice to modify the size of the line memory as taught by Mano et al. corresponding to 400 pixels or 512 pixels since applicant has not disclosed that having the size of line memory corresponding to 400 or 512 pixels solves any stated problem or is for any particular purpose because the size of line memory will vary based on the amount of data being processed or displayed and it appears that any memory size would perform equally well depending upon the amount of data.

7. Claims 3, 4, 9, 11, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mano et al. (U.S. Patent No. 4,985,698) in view of Kubota et al. (U.S. Patent No. 5,977,944).

Referring to claims 3, 4, and 11, Mano et al. teach all the limitations of claim 3 as applied to claims 1 and 10 above, except for the input-side and output-side line memories are n-stage shift registers, and an input data switching circuit for switch output transferred data.

However, Kubota et al. teach a data signal output circuit which is divided into a plurality of blocks includes: a shift register for shifting a scanning signal one after another so as to output the scanning signal in synchronism with a clock signal, the shift register being divided into a plurality of parts in accordance with the blocks; a select output unit for making a sampling of an inputted digital signal in synchronism with the scanning signal, and for outputting a data signal corresponding to the digital signal thus sampled to a plurality of output lines, the select output unit being divided into a plurality of parts as the shift register; and a supply circuit, provided in the each block, for supplying the digital signal to a divided part of the select output circuit in the each block at least during a period of time in which the divided part should operate (col. 3, lines 47-63). As shown in Fig. 6, Kubota et al. teach the pulse signals SRP from the shift register sections 21 in the last stages of the blocks BLK1 to BLKn-1 are supplied to the supply circuits 24 of blocks BLK2 to BLKn respectively provided in the following stages. Further, the pulse signals SRP from the shift register sections 21 in the first stages of the blocks BLK2 to BLKn are supplied to the supply circuits 24 of the blocks BLK1 to BLKn-1 respectively provided in the preceding stages of the blocks BLK2 to BLKn (col. 7, lines 37-45).

Therefore, it would have obvious to one skilled in the art to utilize the method of driving output data as taught by Kubota et al. in combination with the driving circuit as taught by Mano et al. so that the digital signal supplied to all the blocks simultaneously is avoided and therefore, the effective load on the signal line for supplying a digital signal can be reduced, thereby greatly reducing the power consumption of thus data signal output circuit (col. 4, lines 1-6).

In regard to claims 9 and 19, as shown in Fig. 24, Kubota et al. teach the transfer circuit 15 transfers the image signal DIG corresponding to one horizontal scanning period during a horizontal blanking period at once (col. 19, lines 43-45).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mano et al. (U.S. Patent No. 4,985,698) in view of Kubota et al. (U.S. Patent No. 5,977,944) further in view of Asada (U.S. Patent No. 6,020,871).

As cited above, Mano et al. and Kubota et al. teach all the limitations of claim 12 as applied to claim 11 above, except for the output-side memory further including a bi-directional shift register.

However, bi-direction shift registers are well known in the art of display as disclosed in US 6,020,871 to Asada. Therefore, it would have been obvious to one skilled in the art to utilize the driving circuits as taught by Mao et al. and Kubota et al. in combination with the shift register as taught by Asada in order to achieve a high speed bi-directional scanning circuit applicable even when a plurality of IC chips are connected in cascade (col. 3, lines 16-18).

8. Claims 13-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

11/14/2002

Matthew C. Bella
Primary Examiner